

Description

The LCE3035Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

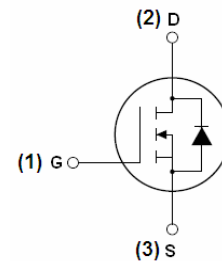
General Features

- $V_{DS} = 30V, I_D = 35A$
 $R_{DS(ON)} < 7.0m\Omega @ V_{GS}=10V$
 $R_{DS(ON)} < 12m\Omega @ V_{GS}=4.5V$
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

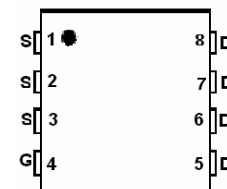
Application

- Secondary side synchronous rectifier
- High side switch in POL DC/DC converter

100% UIS TESTED!



Schematic diagram



DFN 3x3 EP top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
3035Q	LCE3035Q	DFN 3x3 EP	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	35	A
Pulsed Drain Current	I_{DM}	120	A
Maximum Power Dissipation	P_D	35	W
Derating factor		0.28	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	150	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.6	$^{\circ}C/W$
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Electrical Characteristics (TC=25 $^{\circ}C$ unless otherwise noted)

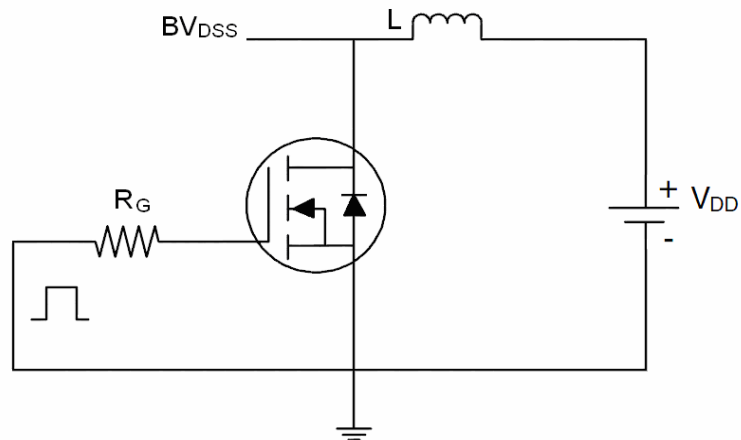
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	33	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$	-	5.9	7.0	m Ω
		$V_{GS}=4.5V, I_D=10A$	-	8.9	12.0	
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=12A$	30	-	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $F=1.0MHz$	-	2330	-	PF
Output Capacitance	C_{oss}		-	460	-	PF
Reverse Transfer Capacitance	C_{rss}		-	230	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=12A$ $V_{GS}=10V, R_{GEN}=6\Omega$	-	18	-	nS
Turn-on Rise Time	t_r		-	10	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	34	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=12A,$ $V_{GS}=10V$	-	45	-	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain Charge	Q_{gd}		-	10	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=12A$	-	0.85	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	35	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 12A$ $di/dt = 100A/\mu s$ ^(Note 3)	-	-	47	nS
Reverse Recovery Charge	Q_{rr}		-	-	25	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

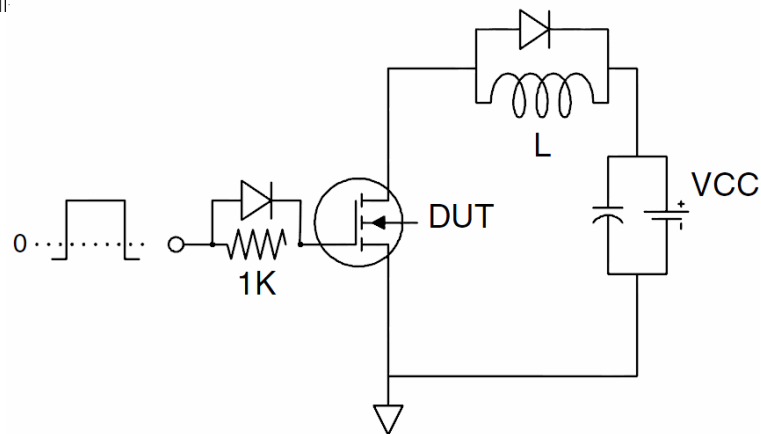
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=15V, V_G=10V, L=0.1mH, R_g=25\Omega$

Test Circuit

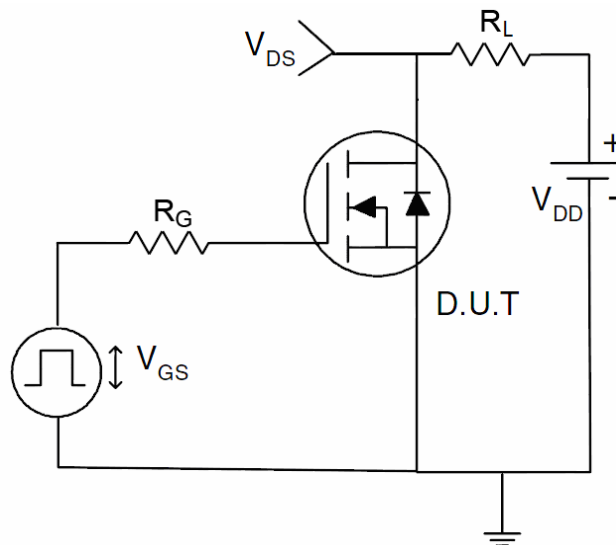
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

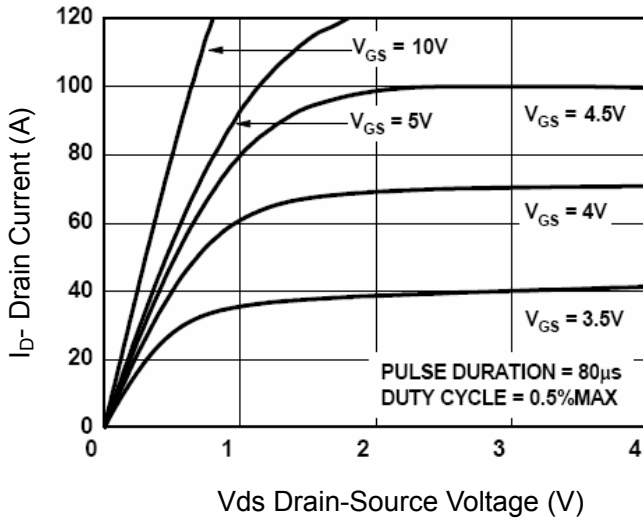


Figure 1 Output Characteristics

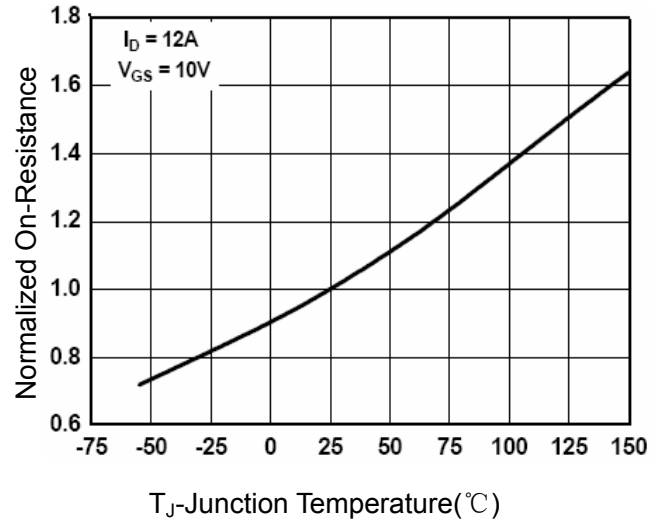


Figure 4 R_{dson} -Junction Temperature

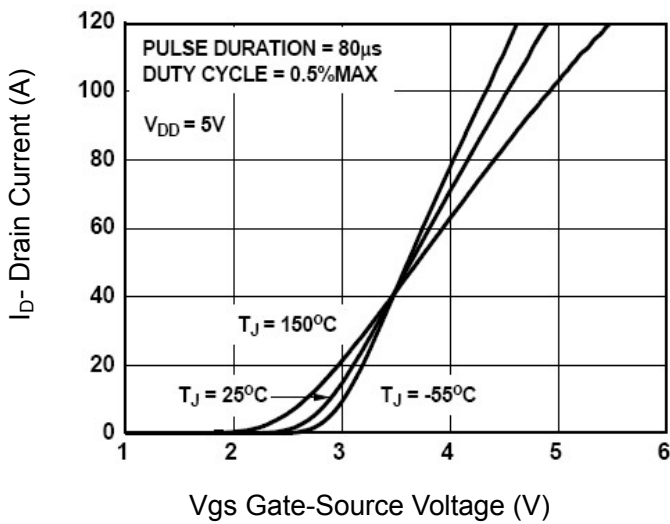


Figure 2 Transfer Characteristics

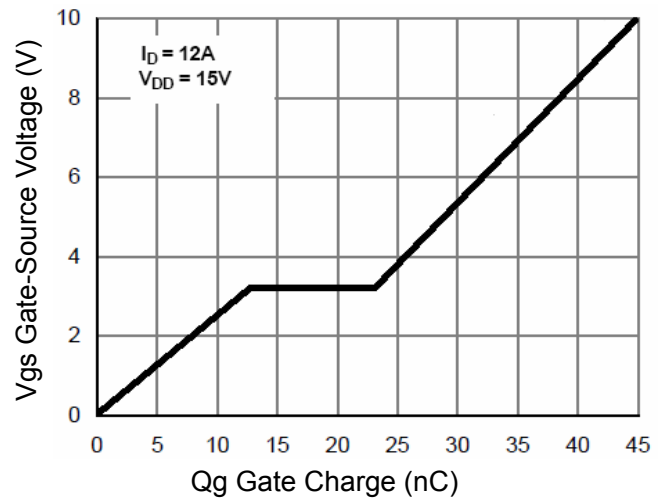


Figure 5 Gate Charge

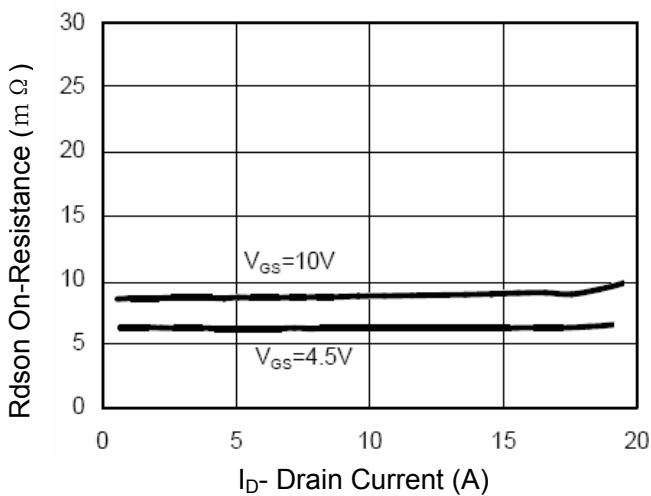


Figure 3 R_{dson} - Drain Current

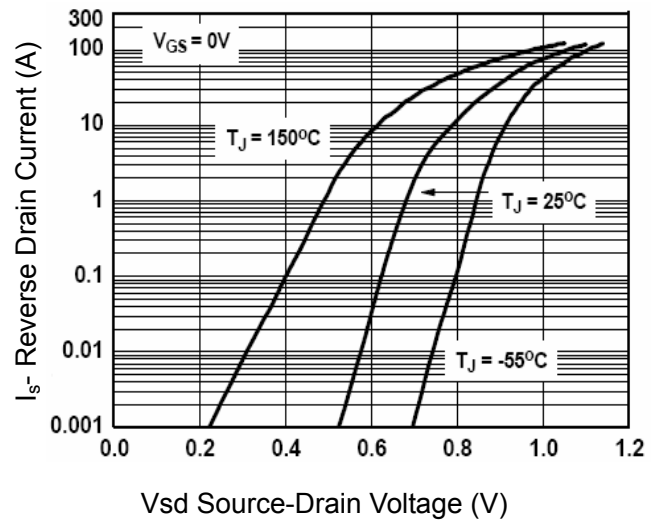


Figure 6 Source- Drain Diode Forward

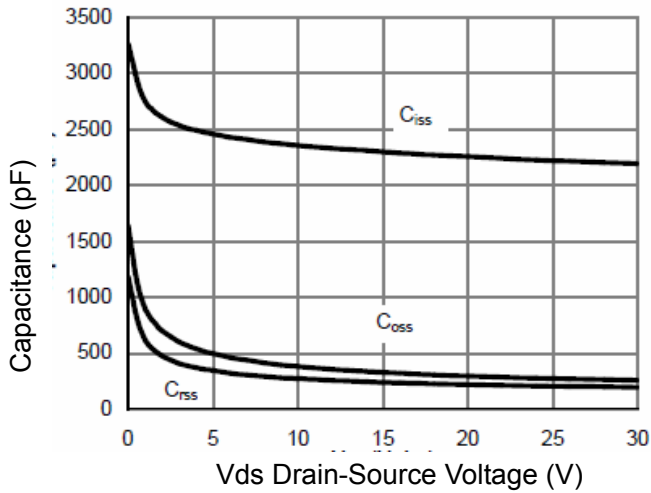


Figure 7 Capacitance vs Vds

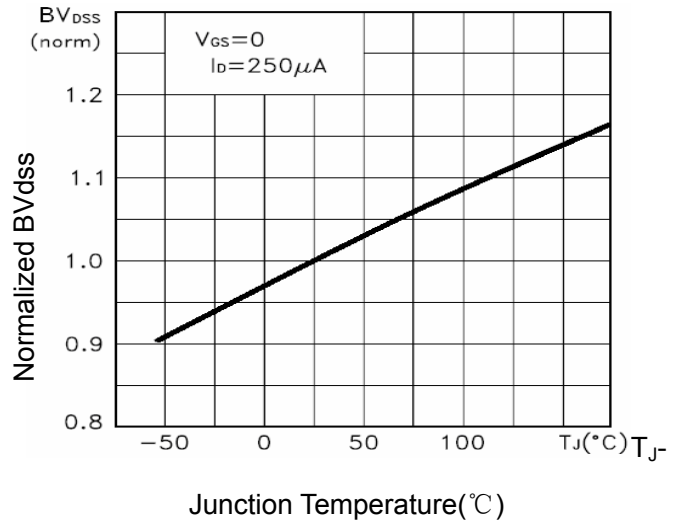


Figure 9 BV_{DSS} vs Junction Temperature

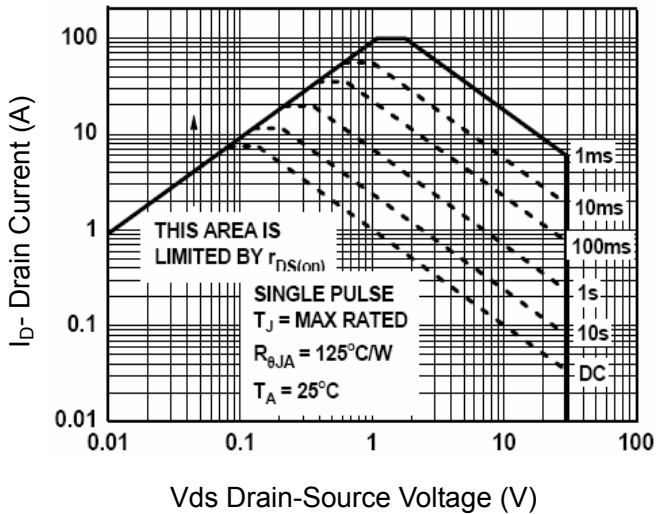


Figure 8 Safe Operation Area

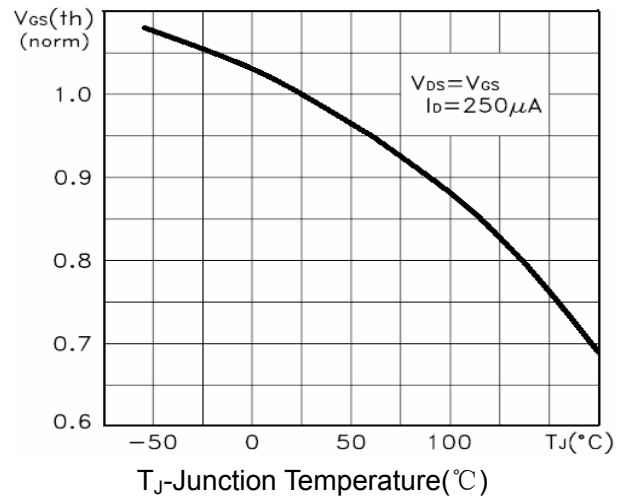


Figure 10 $V_{GS(th)}$ vs Junction Temperature

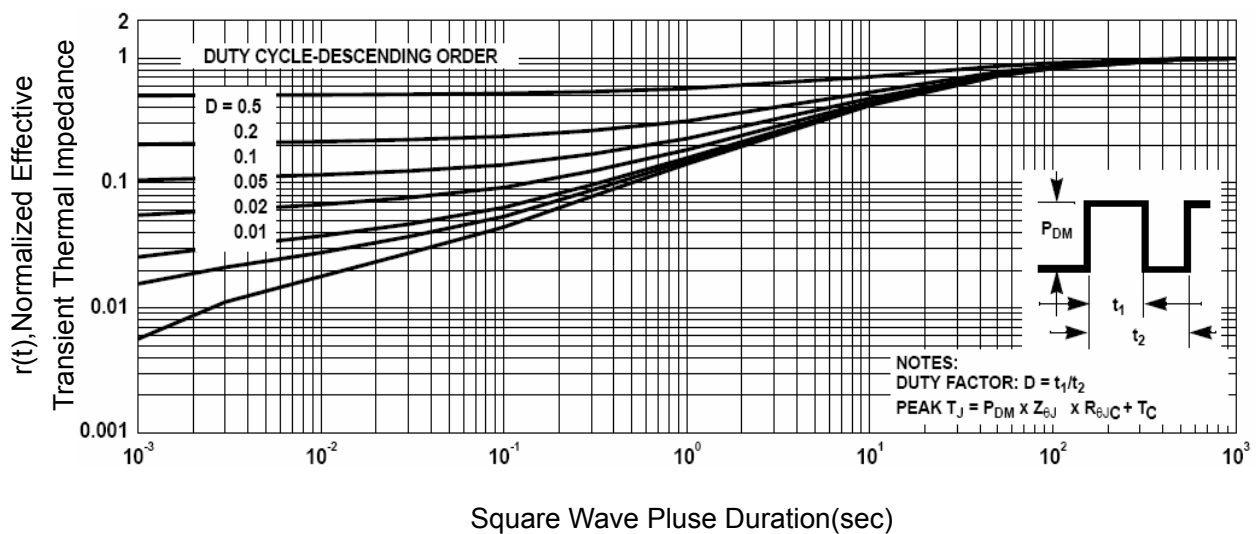
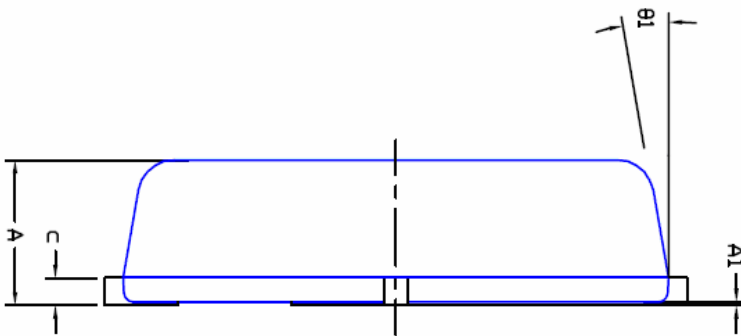
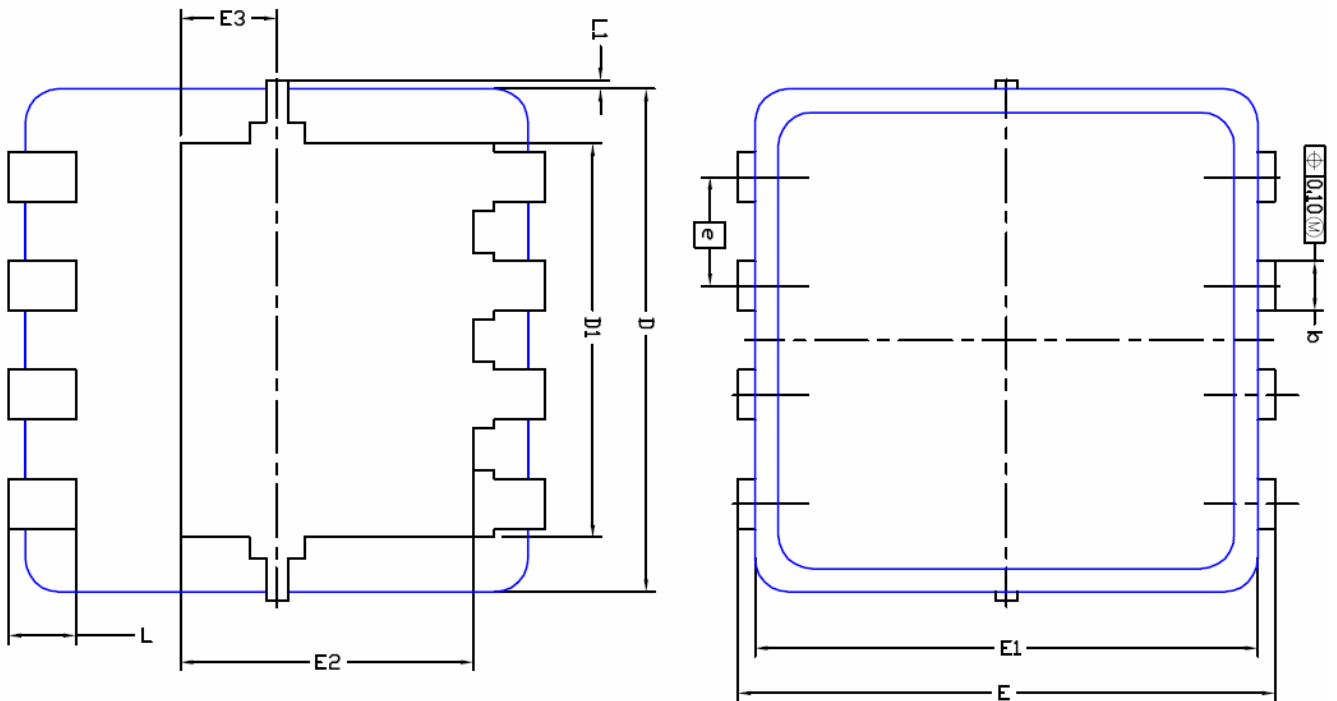


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0,700	0,80	0,900	0,0276	0,0315	0,0354
A1	0,00	---	0,05	0,000	---	0,002
b	0,24	0,30	0,35	0,009	0,012	0,014
c	0,10	0,152	0,25	0,004	0,006	0,010
D	3,00 BSC			0,118 BSC		
D1	2,35 BSC			0,093 BSC		
E	3,20 BSC			0,126 BSC		
E1	3,00 BSC			0,118 BSC		
E2	1,75 BSC			0,069 BSC		
E3	0,575 BSC			0,023 BSC		
e	0,65 BSC			0,026 BSC		
L	0,30	0,40	0,50	0,0118	0,0157	0,0197
L1	0	---	0,100	0	---	0,004
theta	0°	10°	12°	0°	10°	12°